

## AMC1311x High-Impedance, 2-V Input, Reinforced Isolated Amplifiers

### 1 Features

- 2-V, High-Impedance Input Voltage Range  
Optimized for Isolated Voltage Measurement
- Low Offset Error and Drift:
  - AMC1311B:  $\pm 1.5$  mV (max),  $\pm 15$   $\mu$ V/ $^{\circ}$ C (max)
  - AMC1311:  $\pm 9.9$  mV (max),  $\pm 20$   $\mu$ V/ $^{\circ}$ C (typ)
- Fixed Gain: 1
- Very Low Gain Error and Drift:
  - AMC1311B:  $\pm 0.3\%$  (max),  $\pm 45$  ppm/ $^{\circ}$ C (max)
  - AMC1311:  $\pm 1\%$  (max),  $\pm 30$  ppm/ $^{\circ}$ C (typ)
- Low Nonlinearity and Drift: 0.01%, 1 ppm/ $^{\circ}$ C (typ)
- 3.3-V Operation on High-Side (AMC1311B)
- Missing High-Side Supply Indication
- Safety-Related Certifications:
  - 7000-V<sub>PK</sub> Reinforced Isolation per DIN V VDE V 0884-11 (VDE V 0884-11): 2017-01
  - 5000-V<sub>RMS</sub> Isolation for 1 Minute per UL1577
  - CAN/CSA No. 5A-Component Acceptance Service Notice, IEC 60950-1, and IEC 60065 End Equipment Standards

### 2 Applications

- Isolated Voltage Sensing In:
  - Motor Drives
  - Frequency Inverters
  - Uninterruptible Power Supplies

### 3 Description

The AMC1311 device is a precision, isolated amplifier with an output separated from the input circuitry by an isolation barrier that is highly resistant to magnetic interference. This barrier is certified to provide reinforced galvanic isolation of up to 7 kV<sub>PEAK</sub> according to VDE V 0884-11 and UL1577. Used in conjunction with isolated power supplies, this isolated amplifier separates parts of the system that operate on different common-mode voltage levels and protects lower-voltage parts from damage.

The high-impedance input of the AMC1311 is optimized for connection to high-voltage resistive dividers or other voltage signal sources with high output resistance. The excellent performance of the device supports accurate, low temperature drift voltage or temperature sensing and control in closed-loop systems. The integrated missing high-side supply voltage detection feature simplifies system-level design and diagnostics.

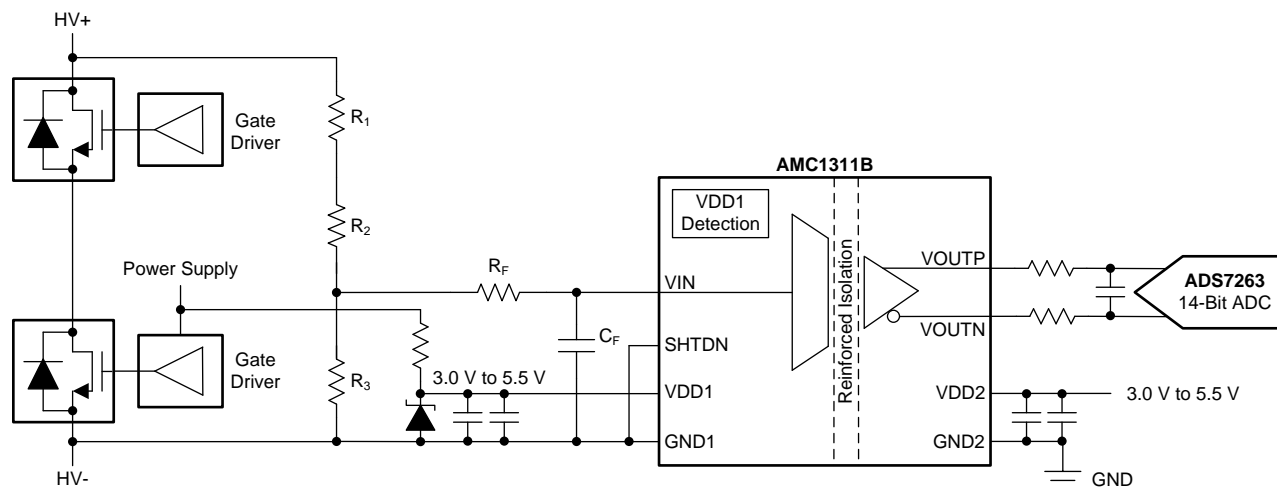
The AMC1311 is offered with two performance grade options: the AMC1311B is specified over the extended industrial temperature range of  $-55^{\circ}$ C to  $+125^{\circ}$ C, and the AMC1311 for operation at  $-40^{\circ}$ C to  $+125^{\circ}$ C.

**Device Information (1)**

PART NUMBER	PACKAGE	BODY SIZE (NOM)
AMC1311x	SOIC (8)	5.85 mm x 7.50 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

### Simplified Schematic



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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

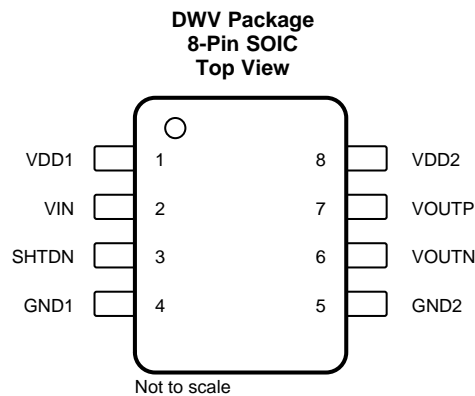
DATE	REVISION	NOTES
December 2017	*	Initial release.



## 5 Device Comparison Table

PARAMETER		AMC1311B	AMC1311
High-side supply voltage, VDD1		3.0 V to 5.5 V	4.5 V to 5.5 V
Specified ambient temperature, T <sub>A</sub>		–55°C to +125°C	–40°C to +125°C
Input offset voltage, V <sub>OS</sub>	4.5 V ≤ VDD1 ≤ 5.5 V	±1.5 mV	±9.9 mV
	3.0 V ≤ VDD1 ≤ 5.5 V	±2.5 mV	Not applicable
Input offset drift, TCV <sub>OS</sub>		±3 μV/°C (typ), ±15 μV/°C (max)	±20 μV/°C (typ)
Gain error, E <sub>G</sub>		±0.3%	±1%
Gain error drift, TCE <sub>G</sub>		±5 ppm/°C (typ), ±45 ppm/°C (max)	±30 ppm/°C (typ)
Common-mode transient immunity, CMTI		75 kV/μs (min)	15 kV/μs (min)

## 6 Pin Configuration and Functions



### Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	VDD1	—	High-side power supply, 3.0 V to 5.5 V for the AMC1311B (4.5 V to 5.5 V for the AMC1311), relative to GND1. See the <a href="#">Power Supply Recommendations</a> section for power-supply decoupling recommendations.
2	VIN	I	Analog input
3	SHTDN	I	Shutdown input, active high, with internal pullup resistor (typical value: 100 kΩ)
4	GND1	—	High-side analog ground
5	GND2	—	Low-side analog ground
6	VOUTN	O	Inverting analog output
7	VOUTP	O	Noninverting analog output
8	VDD2	—	Low-side power supply, 3.0 V to 5.5 V, relative to GND2. See the <a href="#">Power Supply Recommendations</a> section for power-supply decoupling recommendations.



## 7 Specifications

### 7.1 Absolute Maximum Ratings<sup>(1)</sup>

		MIN	MAX	UNIT
Power-supply voltage	VDD1 to GND1	−0.3	6.5	V
	VDD2 to GND2	−0.3	6.5	
Input voltage	VIN	GND1 − 6	VDD1 + 0.5	V
	SHTDN	GND1 − 0.5	VDD1 + 0.5	
Output voltage	VOUTP, VOUTN	GND2 − 0.5	VDD2 + 0.5	V
Input current	Continuous, any pin except power-supply pins	−10	10	mA
Temperature	Junction, T <sub>J</sub>		150	°C
	Storage, T <sub>stg</sub>	−65	150	

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 7.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub> Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 7.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
<b>POWER SUPPLY</b>					
High-side power supply	VDD1 to GND1, AMC1311	4.5	5	5.5	V
	VDD1 to GND1, AMC1311B	3.0	5	5.5	
Low-side power supply	VDD2 to GND2	3.0	3.3	5.5	V
<b>ANALOG INPUT</b>					
Absolute input voltage	VIN to GND1	−2		VDD1	V
V <sub>FSR</sub> Specified linear input full-scale voltage	VIN to GND1	−0.1		2	V
V <sub>Clipping</sub> Input voltage before clipping output	VIN to GND1		2.516		V
<b>DIGITAL INPUT</b>					
Input voltage	SHTDN	GND1		VDD1	V
<b>TEMPERATURE RANGE</b>					
T <sub>A</sub> Specified ambient temperature	AMC1311	−40		125	°C
	AMC1311B	−55		125	



## 7.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		AMC1311x	UNIT
		DWV (SOIC)	
		8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	84.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	28.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	41.1	°C/W
$\psi_{JT}$	Junction-to-top characterization parameter	4.9	°C/W
$\psi_{JB}$	Junction-to-board characterization parameter	39.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 7.5 Power Ratings

PARAMETER		TEST CONDITIONS	VALUE	UNIT
$P_D$	Maximum power dissipation (both sides)	VDD1 = VDD2 = 5.5 V	97.9	mW
		VDD1 = VDD2 = 3.6 V, AMC1311B only	56.16	
$P_{D1}$	Maximum power dissipation (high-side supply)	VDD1 = 5.5 V	53.35	mW
		VDD1 = 3.6 V, AMC1311B only	30.24	
$P_{D2}$	Maximum power dissipation (low-side supply)	VDD2 = 5.5 V	44.55	mW
		VDD2 = 3.6 V	25.92	



## 7.6 Insulation Specifications

over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	VALUE	UNIT
GENERAL				
CLR	External clearance <sup>(1)</sup>	Shortest pin-to-pin distance through air	≥ 9	mm
CPG	External creepage <sup>(1)</sup>	Shortest pin-to-pin distance across the package surface	≥ 9	mm
DTI	Distance through insulation	Minimum internal gap (internal clearance) of the double insulation (2 × 0.0105 mm)	≥ 0.021	mm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	≥ 600	V
	Material group	According to IEC 60664-1	I	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 300 V <sub>RMS</sub>	I-IV	
		Rated mains voltage ≤ 600 V <sub>RMS</sub>	I-IV	
		Rated mains voltage ≤ 1000 V <sub>RMS</sub>	I-III	
DIN V VDE V 0884-11 (VDE V 0884-11): 2017-01 <sup>(2)</sup>				
V <sub>IORM</sub>	Maximum repetitive peak isolation voltage	At ac voltage (bipolar)	2121	V <sub>PK</sub>
V <sub>IOWM</sub>	Maximum-rated isolation working voltage	At ac voltage (sine wave)	1500	V <sub>RMS</sub>
		At dc voltage	2121	V <sub>DC</sub>
V <sub>IOTM</sub>	Maximum transient isolation voltage	V <sub>TEST</sub> = V <sub>IOTM</sub> , t = 60 s (qualification test)	7000	V <sub>PK</sub>
		V <sub>TEST</sub> = 1.2 × V <sub>IOTM</sub> , t = 1 s (100% production test)	8400	
V <sub>IOSM</sub>	Maximum surge isolation voltage <sup>(3)</sup>	Test method per IEC 60065, 1.2/50-μs waveform, V <sub>TEST</sub> = 1.6 × V <sub>IOSM</sub> = 12800 V <sub>PK</sub> (qualification)	8000	V <sub>PK</sub>
q <sub>pd</sub>	Apparent charge <sup>(4)</sup>	Method a, after input/output safety test subgroup 2 / 3, V <sub>ini</sub> = V <sub>IOTM</sub> , t <sub>ini</sub> = 60 s, V <sub>pd(m)</sub> = 1.2 × V <sub>IORM</sub> = 2545 V <sub>PK</sub> , t <sub>m</sub> = 10 s	≤ 5	pC
		Method a, after environmental tests subgroup 1, V <sub>ini</sub> = V <sub>IOTM</sub> , t <sub>ini</sub> = 60 s, V <sub>pd(m)</sub> = 1.6 × V <sub>IORM</sub> = 3394 V <sub>PK</sub> , t <sub>m</sub> = 10 s	≤ 5	
		Method b1, at routine test (100% production) and preconditioning (type test), V <sub>ini</sub> = V <sub>IOTM</sub> , t <sub>ini</sub> = 1 s, V <sub>pd(m)</sub> = 1.875 × V <sub>IORM</sub> = 3977 V <sub>PK</sub> , t <sub>m</sub> = 1 s	≤ 5	
C <sub>IO</sub>	Barrier capacitance, input to output <sup>(5)</sup>	V <sub>IO</sub> = 0.5 V <sub>PP</sub> at 1 MHz	~1	pF
R <sub>IO</sub>	Insulation resistance, input to output <sup>(5)</sup>	V <sub>IO</sub> = 500 V at T <sub>A</sub> = 25°C	> 10 <sup>12</sup>	Ω
		V <sub>IO</sub> = 500 V at 100°C ≤ T <sub>A</sub> ≤ 125°C	> 10 <sup>11</sup>	
		V <sub>IO</sub> = 500 V at T <sub>S</sub> = 150°C	> 10 <sup>9</sup>	
	Pollution degree		2	
	Climatic category		55/125/21	
UL1577				
V <sub>ISO</sub>	Withstand isolation voltage	V <sub>TEST</sub> = V <sub>ISO</sub> = 5000 V <sub>RMS</sub> or 7000 V <sub>DC</sub> , t = 60 s (qualification), V <sub>TEST</sub> = 1.2 × V <sub>ISO</sub> = 6000 V <sub>RMS</sub> , t = 1 s (100% production test)	5000	V <sub>RMS</sub>

- (1) Apply creepage and clearance requirements according to the specific equipment isolation standards of an application. Care must be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed circuit board (PCB) do not reduce this distance. Creepage and clearance on a PCB become equal in certain cases. Techniques such as inserting grooves and ribs on the PCB are used to help increase these specifications.
- (2) This coupler is suitable for *safe electrical insulation* only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
- (3) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
- (4) Apparent charge is electrical discharge caused by a partial discharge (pd).
- (5) All pins on each side of the barrier are tied together, creating a two-pin device.



## 7.7 Safety-Related Certifications

VDE	UL
Certified according to DIN V VDE V 0884-11 (VDE V 0884-11): 2017-01, DIN EN 60950-1 (VDE 0805 Teil 1): 2014-08, and DIN EN 60065 (VDE 0860): 2005-11	Recognized under 1577 component recognition and CSA component acceptance NO 5 programs
Reinforced insulation	Single protection
Certificate number: 40040142	File number: E181974

## 7.8 Safety Limiting Values

Safety limiting intends to minimize potential damage to the isolation barrier upon failure of input or output (I/O) circuitry. A failure of the I/O may allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier, potentially leading to secondary system failures.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I <sub>S</sub> Safety input, output, or supply current	R <sub>θJA</sub> = 84.6°C/W, T <sub>J</sub> = 150°C, T <sub>A</sub> = 25°C, VDD1 = VDD2 = 5.5 V, see <a href="#">Figure 2</a>			268	mA
	R <sub>θJA</sub> = 84.6°C/W, T <sub>J</sub> = 150°C, T <sub>A</sub> = 25°C, VDD1 = VDD2 = 3.6 V, AMC1311B only, see <a href="#">Figure 2</a>			410	
P <sub>S</sub> Safety input, output, or total power <sup>(1)</sup>	R <sub>θJA</sub> = 84.6°C/W, T <sub>J</sub> = 150°C, T <sub>A</sub> = 25°C, see <a href="#">Figure 3</a>			1477	mW
T <sub>S</sub> Maximum safety temperature				150	°C

(1) Input, output, or the sum of input and output power must not exceed this value.

The maximum safety temperature is the maximum junction temperature specified for the device. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determines the junction temperature. The assumed junction-to-air thermal resistance in the [Thermal Information](#) table is that of a device installed on a high-K test board for leaded surface-mount packages. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance.



## 7.9 Electrical Characteristics

minimum and maximum specifications of the AMC1311 apply from  $T_A = -40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ ,  $V_{DD1} = 4.5\text{ V}$  to  $5.5\text{ V}$ ,  $V_{DD2} = 3.0\text{ V}$  to  $5.5\text{ V}$ ,  $V_{IN} = -0.1\text{ V}$  to  $2\text{ V}$ , and  $\text{SHTDN} = \text{GND1} = 0\text{ V}$ ; minimum and maximum specifications of the AMC1311B apply from  $T_A = -55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ ,  $V_{DD1} = 3.0\text{ V}$  to  $5.5\text{ V}$ ,  $V_{DD2} = 3.0\text{ V}$  to  $5.5\text{ V}$ ,  $V_{IN} = -0.1\text{ V}$  to  $2\text{ V}$ , and  $\text{SHTDN} = \text{GND1} = 0\text{ V}$ ; typical specifications are at  $T_A = 25^{\circ}\text{C}$ ,  $V_{DD1} = 5\text{ V}$ , and  $V_{DD2} = 3.3\text{ V}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>ANALOG INPUT</b>						
$V_{OS}$	Input offset voltage <sup>(1)</sup>	AMC1311, initial, at $T_A = 25^{\circ}\text{C}$ , $V_{IN} = \text{GND1}$	-9.9	$\pm 0.4$	9.9	mV
		AMC1311B, initial, at $T_A = 25^{\circ}\text{C}$ , $V_{IN} = \text{GND1}$ , $4.5\text{ V} \leq V_{DD1} \leq 5.5\text{ V}$	-1.5	$\pm 0.4$	1.5	
		AMC1311B, initial, at $T_A = 25^{\circ}\text{C}$ , $V_{IN} = \text{GND1}$ , $3.0\text{ V} \leq V_{DD1} \leq 5.5\text{ V}$ <sup>(2)</sup>	-2.5	-1.1	2.5	
$\text{TCV}_{OS}$	Input offset drift <sup>(1)</sup>	AMC1311		$\pm 20$		$\mu\text{V}/^{\circ}\text{C}$
		AMC1311B	-15	$\pm 3$	15	
$C_{IN}$	Input capacitance <sup>(3)</sup>	$f_{IN} = 275\text{ kHz}$		7		pF
$R_{IN}$	Input resistance <sup>(3)</sup>			1		G $\Omega$
$I_{IB}$	Input bias current	$V_{IN} = \text{GND1}$	-15	3.5	15	nA
$\text{TCI}_{IB}$	Input bias current drift			$\pm 10$		$\mu\text{A}/^{\circ}\text{C}$
<b>ANALOG OUTPUT</b>						
	Nominal gain			1		
$E_G$	Gain error <sup>(1)</sup>	AMC1311, initial, at $T_A = 25^{\circ}\text{C}$	-1%	0.4%	1%	
		AMC1311B, initial, at $T_A = 25^{\circ}\text{C}$	-0.3%	$\pm 0.05\%$	0.3%	
$\text{TCE}_G$	Gain error drift <sup>(1)</sup>	AMC1311		$\pm 30$		ppm/ $^{\circ}\text{C}$
		AMC1311B	-45	$\pm 5$	45	
	Nonlinearity <sup>(1)</sup>		-0.04%	$\pm 0.01\%$	0.04%	
	Nonlinearity drift			1		ppm/ $^{\circ}\text{C}$
$\text{THD}$	Total harmonic distortion	$V_{IN} = 2\text{ V}$ , $f_{IN} = 10\text{ kHz}$ , $\text{BW} = 100\text{ kHz}$		-87		dB
	Output noise	$V_{IN} = \text{GND1}$ , $\text{BW} = 100\text{ kHz}$		220		$\mu\text{V}_{\text{RMS}}$
$\text{SNR}$	Signal-to-noise ratio	$V_{IN} = 2\text{ V}$ , $f_{IN} = 1\text{ kHz}$ , $\text{BW} = 10\text{ kHz}$	79	82.6		dB
		$V_{IN} = 2\text{ V}$ , $f_{IN} = 10\text{ kHz}$ , $\text{BW} = 100\text{ kHz}$		70.9		
$\text{PSRR}$	Power-supply rejection ratio <sup>(4)</sup>	PSRR vs $V_{DD1}$ , at dc		-65		dB
		PSRR vs $V_{DD1}$ , 100-mV and 10-kHz ripple		-65		
		PSRR vs $V_{DD2}$ , at dc		-85		
		PSRR vs $V_{DD2}$ , 100-mV and 10-kHz ripple		-70		
$V_{\text{CMout}}$	Common-mode output voltage		1.39	1.44	1.49	V
$V_{\text{FAILSAFE}}$	Failsafe differential output voltage	$\text{VOUTP} - \text{VOUTN}$ , $\text{SHTDN} = \text{high}$ , or $V_{DD1} \leq V_{DD1_{\text{UV}}}$ , or $V_{DD1}$ missing		-2.6	-2.5	V
$\text{BW}$	Output bandwidth	AMC1311	100	220		kHz
		AMC1311B	220	275		
$R_{\text{OUT}}$	Output resistance	On $\text{VOUTP}$ or $\text{VOUTN}$		< 0.2		$\Omega$
	Output short-circuit current			$\pm 13$		mA
$\text{CMTI}$	Common-mode transient immunity	$ \text{GND1} - \text{GND2}  = 1\text{ kV}$ , AMC1311	15	30		kV/ $\mu\text{s}$
		$ \text{GND1} - \text{GND2}  = 1\text{ kV}$ , AMC1311B	75	140		

(1) The typical value includes one sigma statistical variation.

(2) The typical value is at  $V_{DD1} = 3.3\text{ V}$ .

(3) Also see the [Analog Input](#) section for more details.

(4) This parameter is output referred.



## Electrical Characteristics (continued)

minimum and maximum specifications of the AMC1311 apply from  $T_A = -40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ ,  $V_{DD1} = 4.5\text{ V}$  to  $5.5\text{ V}$ ,  $V_{DD2} = 3.0\text{ V}$  to  $5.5\text{ V}$ ,  $V_{IN} = -0.1\text{ V}$  to  $2\text{ V}$ , and  $\text{SHTDN} = \text{GND1} = 0\text{ V}$ ; minimum and maximum specifications of the AMC1311B apply from  $T_A = -55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ ,  $V_{DD1} = 3.0\text{ V}$  to  $5.5\text{ V}$ ,  $V_{DD2} = 3.0\text{ V}$  to  $5.5\text{ V}$ ,  $V_{IN} = -0.1\text{ V}$  to  $2\text{ V}$ , and  $\text{SHTDN} = \text{GND1} = 0\text{ V}$ ; typical specifications are at  $T_A = 25^{\circ}\text{C}$ ,  $V_{DD1} = 5\text{ V}$ , and  $V_{DD2} = 3.3\text{ V}$  (unless otherwise noted)

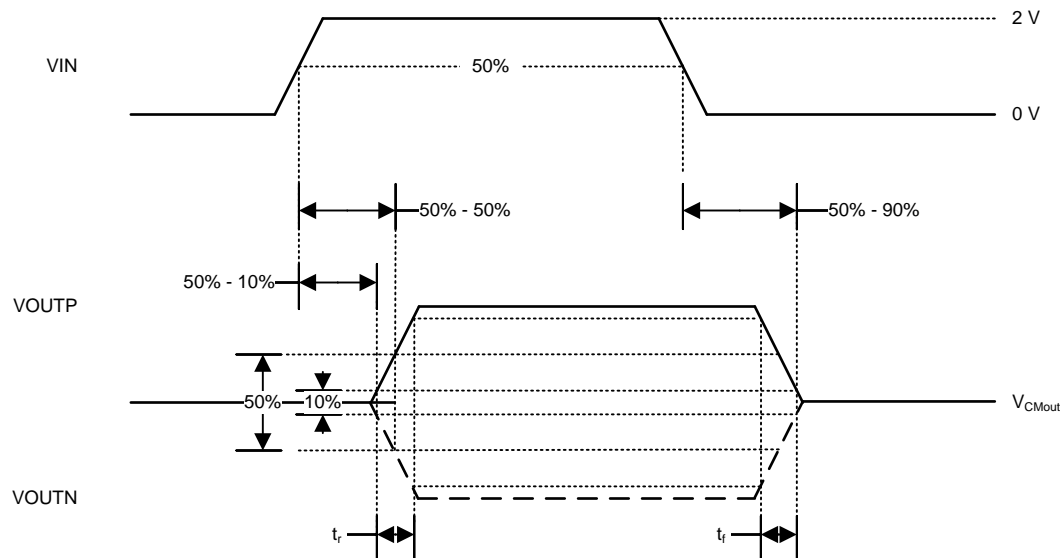
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>DIGITAL INPUT (SHTDN Pin: CMOS Logic Family, CMOS With Schmitt-Trigger)</b>						
$I_{IN}$	Input current	$\text{GND1} \leq V_{\text{SHTDN}} \leq V_{DD1}$	–70		1	$\mu\text{A}$
$C_{IN}$	Input capacitance			5		$\text{pF}$
$V_{IH}$	High-level input voltage		$0.7 \times V_{DD1}$		$V_{DD1} + 0.3$	$\text{V}$
$V_{IL}$	Low-level input voltage		–0.3		$0.3 \times V_{DD1}$	$\text{V}$
<b>POWER SUPPLY</b>						
$V_{DD1UV}$	$V_{DD1}$ undervoltage detection threshold voltage	$V_{DD1}$ falling	1.75	2.53	2.7	$\text{V}$
$I_{DD1}$	High-side supply current	AMC1311B only, $3.0\text{ V} \leq V_{DD1} \leq 3.6\text{ V}$ , $\text{SHTDN} = \text{low}$		6	8.4	$\text{mA}$
		$4.5\text{ V} \leq V_{DD1} \leq 5.5\text{ V}$ , $\text{SHTDN} = \text{low}$		7.1	9.7	
		$\text{SHTDN} = \text{high}$		1.3		$\mu\text{A}$
$I_{DD2}$	Low-side supply current	$3.0\text{ V} \leq V_{DD2} \leq 3.6\text{ V}$		5.3	7.2	$\text{mA}$
		$4.5\text{ V} \leq V_{DD2} \leq 5.5\text{ V}$		5.9	8.1	



## 7.10 Switching Characteristics

over operating ambient temperature range (unless otherwise noted)

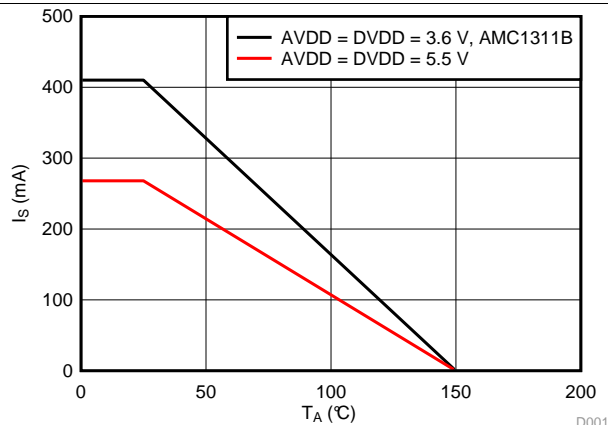
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t <sub>r</sub>	Rise time of VOUTP, VOUTN	See <a href="#">Figure 1</a>		1.3		μs
t <sub>f</sub>	Fall time of VOUTP, VOUTN	See <a href="#">Figure 1</a>		1.3		μs
	VIN to VOUTN, VOUTP signal delay (50% – 10%)	AMC1311, unfiltered output, see <a href="#">Figure 1</a>		1.5	2.5	μs
		AMC1311B, unfiltered output, see <a href="#">Figure 1</a>		1.0	1.5	
	VIN to VOUTN, VOUTP signal delay (50% – 50%)	AMC1311, unfiltered output, see <a href="#">Figure 1</a>		2.1	3.1	μs
		AMC1311B, unfiltered output, see <a href="#">Figure 1</a>		1.6	2.1	
	VIN to VOUTN, VOUTP signal delay (50% – 90%)	AMC1311, unfiltered output, see <a href="#">Figure 1</a>		3.0	4.0	μs
		AMC1311B, unfiltered output, see <a href="#">Figure 1</a>		2.5	3.0	
t <sub>AS</sub>	Analog settling time	VDD1 step to 3.0 V with VDD2 ≥ 3.0 V, to VOUTP, VOUTN valid, 0.1% settling		50	100	μs
t <sub>EN</sub>	Device enable time	SHTDN high to low		50	100	μs
t <sub>SHTDN</sub>	Shutdown time	SHTDN low to high		3	10	μs



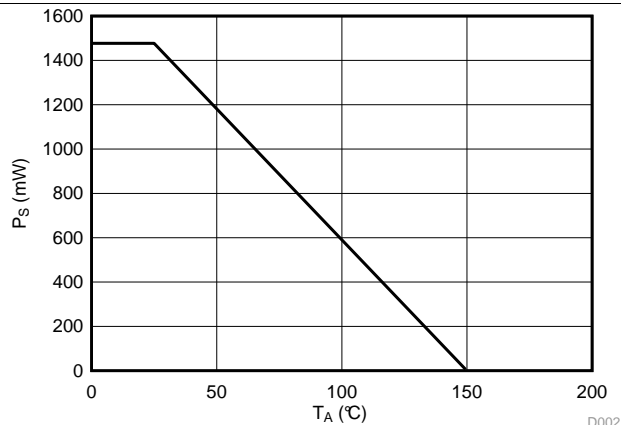
**Figure 1. Rise, Fall, and Delay Time Waveforms**



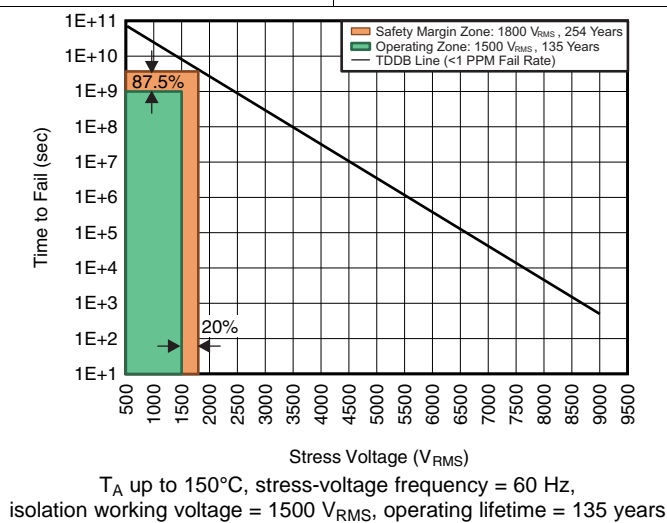
## 7.11 Insulation Characteristics Curves



**Figure 2. Thermal Derating Curve for Safety-Limiting Current per VDE**



**Figure 3. Thermal Derating Curve for Safety-Limiting Power per VDE**

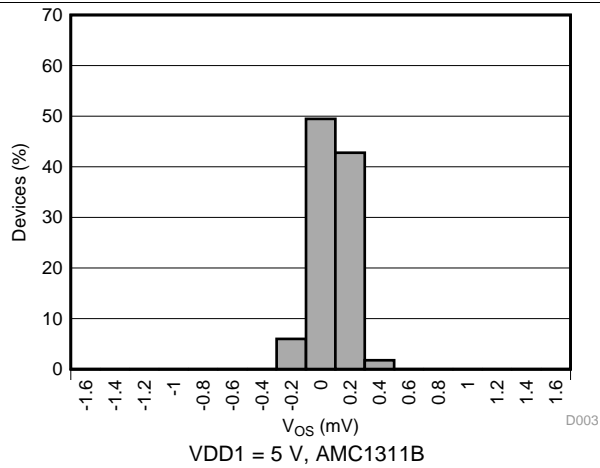


**Figure 4. Reinforced Isolation Capacitor Lifetime Projection**

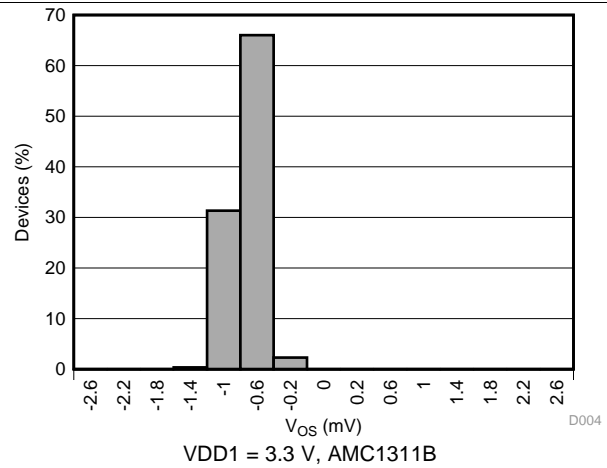


## 7.12 Typical Characteristics

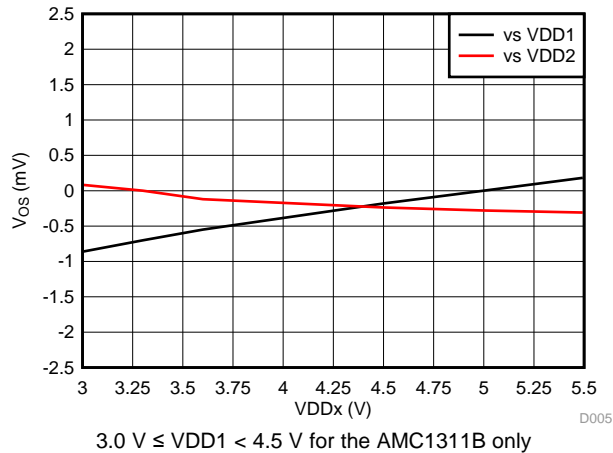
at VDD1 = 5 V, VDD2 = 3.3 V, SHTDN = 0 V,  $f_{IN}$  = 10 kHz, and BW = 100 kHz (unless otherwise noted)



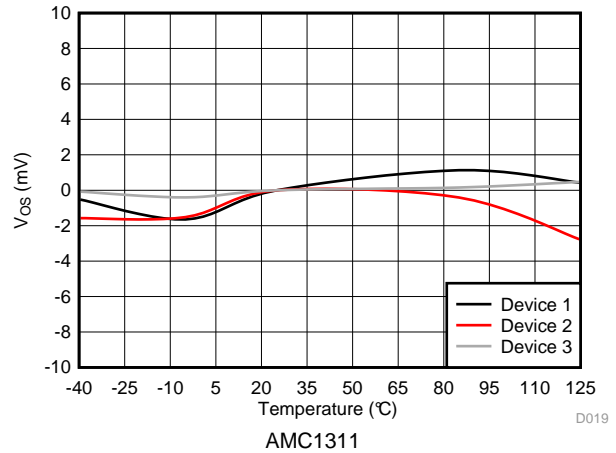
**Figure 5. Input Offset Voltage Histogram**



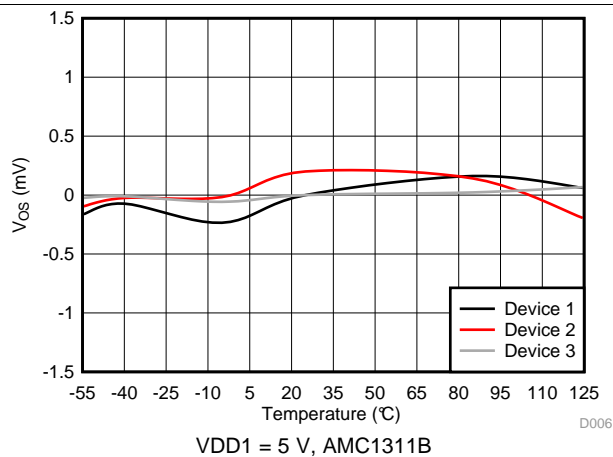
**Figure 6. Input Offset Voltage Histogram**



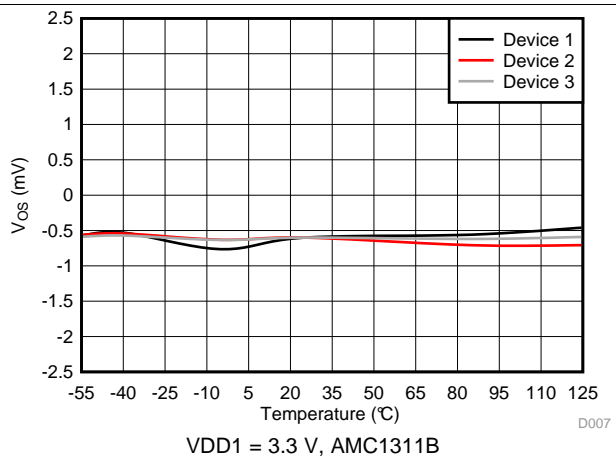
**Figure 7. Input Offset Voltage vs Supply Voltage**



**Figure 8. Input Offset Voltage vs Temperature**



**Figure 9. Input Offset Voltage vs Temperature**

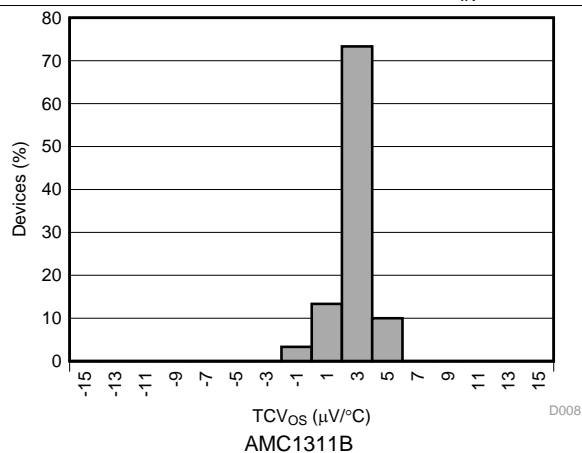


**Figure 10. Input Offset Voltage vs Temperature**

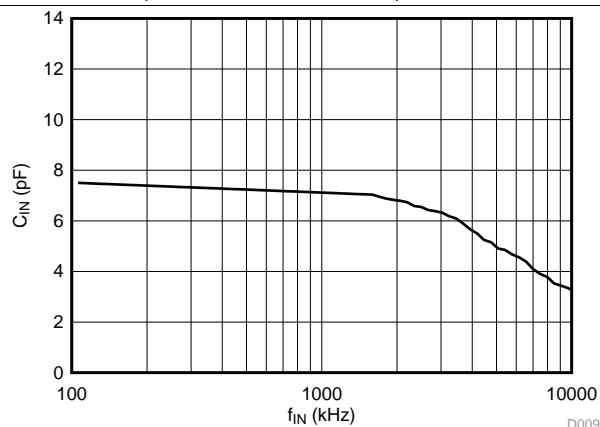


## Typical Characteristics (continued)

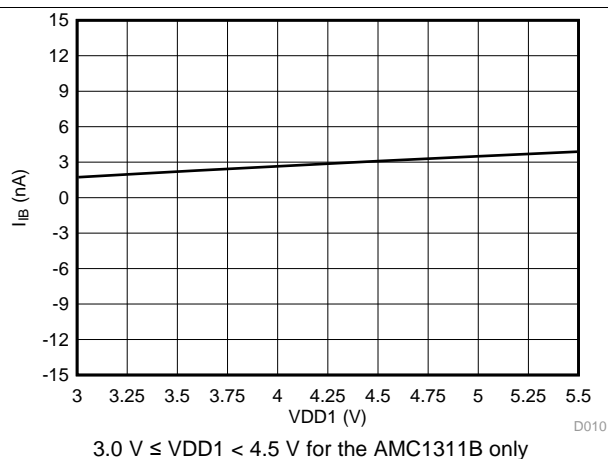
at VDD1 = 5 V, VDD2 = 3.3 V, SHTDN = 0 V,  $f_{IN} = 10$  kHz, and BW = 100 kHz (unless otherwise noted)



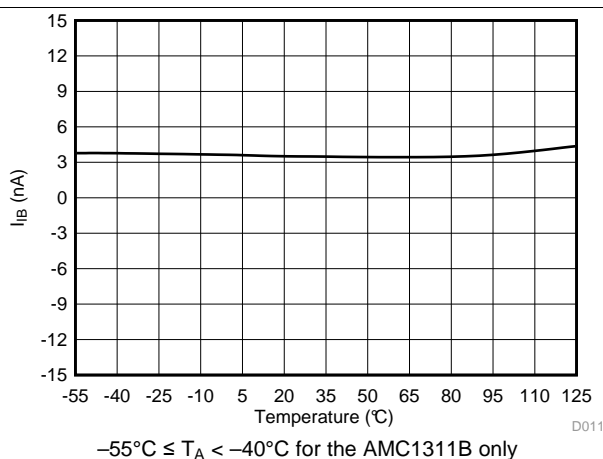
**Figure 11. Input Offset Drift Histogram**



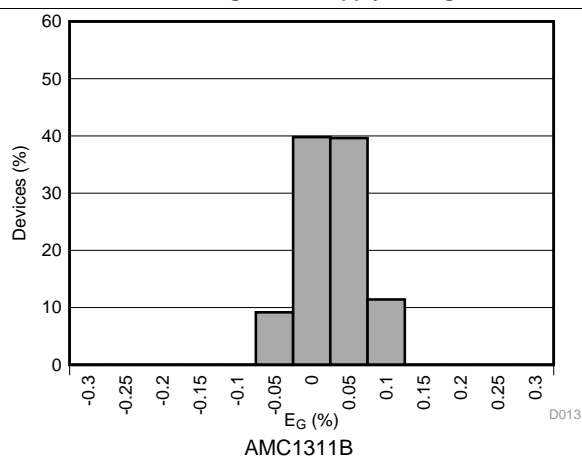
**Figure 12. Input Capacitance vs Input Signal Frequency**



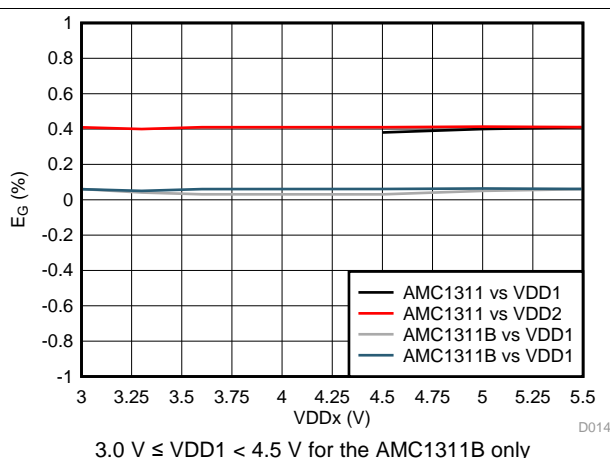
**Figure 13. Input Bias Current vs High-Side Supply Voltage**



**Figure 14. Input Bias Current vs Temperature**



**Figure 15. Gain Error Histogram**



**Figure 16. Gain Error vs Supply Voltage**



## Typical Characteristics (continued)

at  $V_{DD1} = 5\text{ V}$ ,  $V_{DD2} = 3.3\text{ V}$ ,  $SHTDN = 0\text{ V}$ ,  $f_{IN} = 10\text{ kHz}$ , and  $BW = 100\text{ kHz}$  (unless otherwise noted)

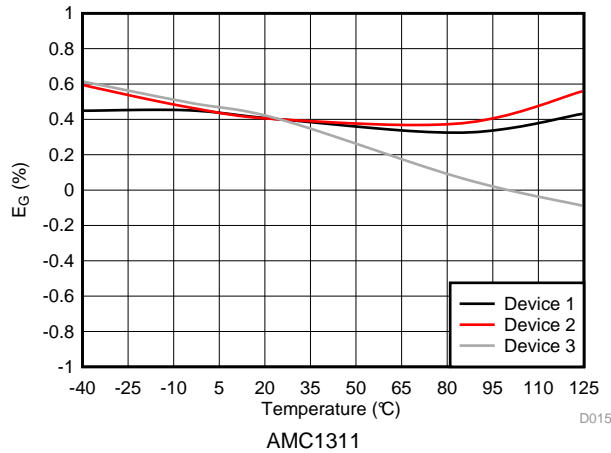


Figure 17. Gain Error vs Temperature

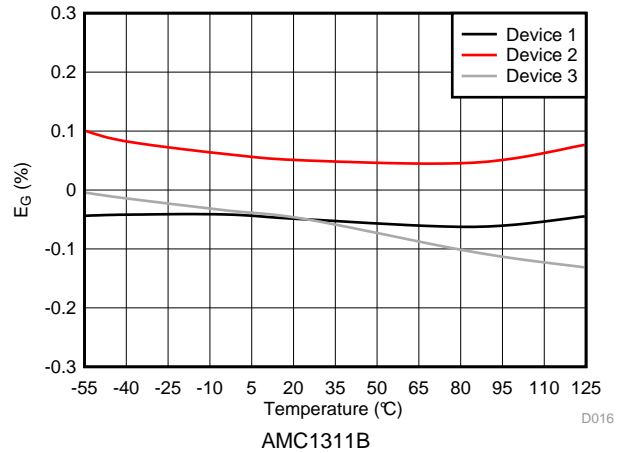


Figure 18. Gain Error vs Temperature

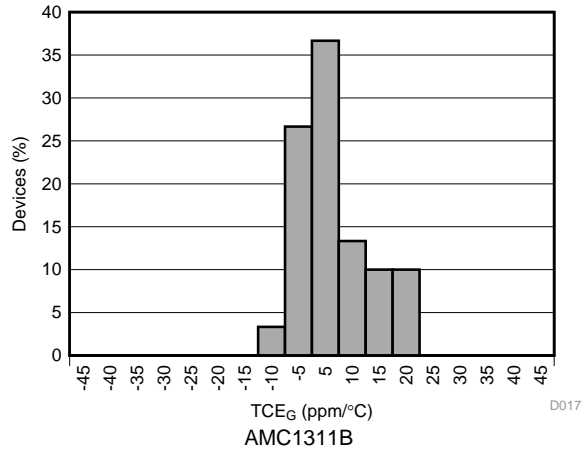


Figure 19. Gain Error Drift Histogram

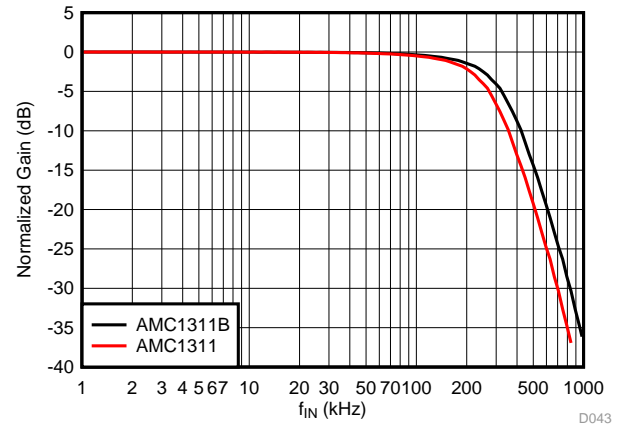


Figure 20. Normalized Gain vs Input Frequency

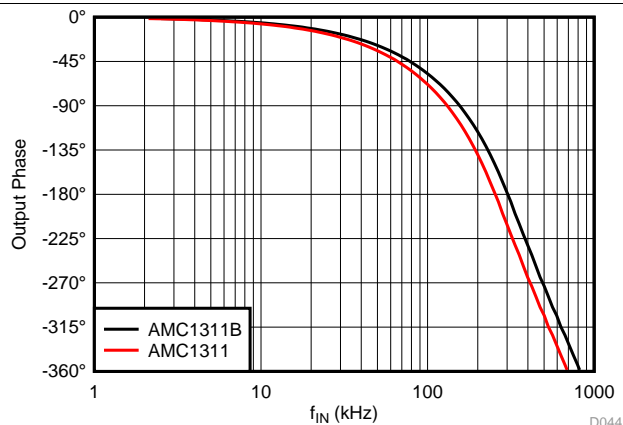


Figure 21. Output Phase vs Input Frequency

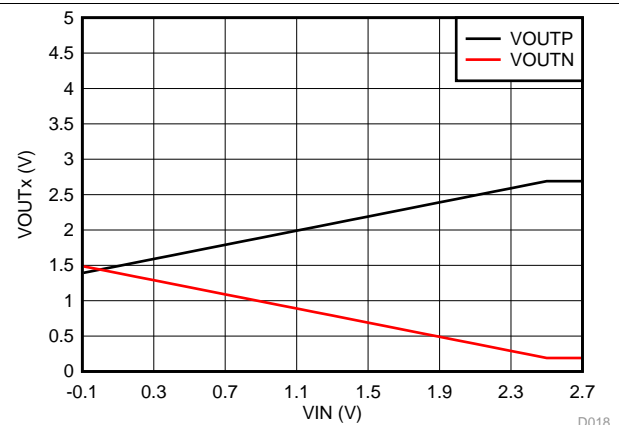
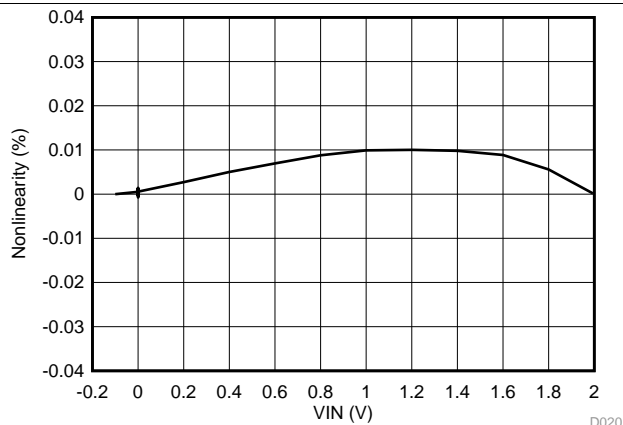


Figure 22. Output Voltage vs Input Voltage

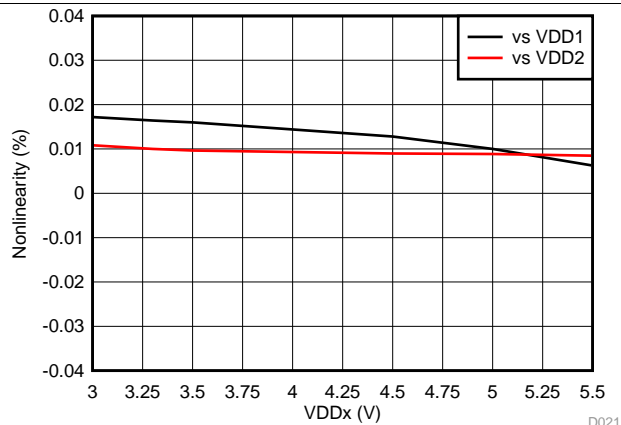


## Typical Characteristics (continued)

at VDD1 = 5 V, VDD2 = 3.3 V, SHTDN = 0 V,  $f_{IN}$  = 10 kHz, and BW = 100 kHz (unless otherwise noted)

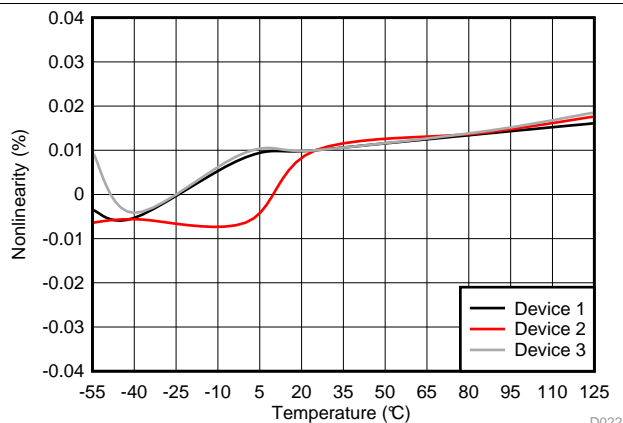


**Figure 23. Nonlinearity vs Input Voltage**



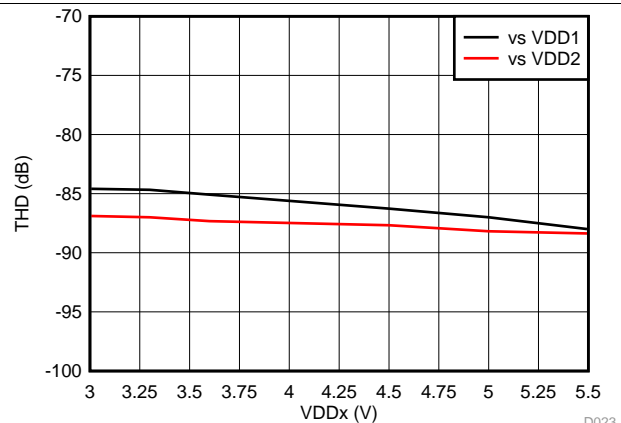
3.0 V ≤ VDD1 < 4.5 V for the AMC1311B only

**Figure 24. Nonlinearity vs Supply Voltage**



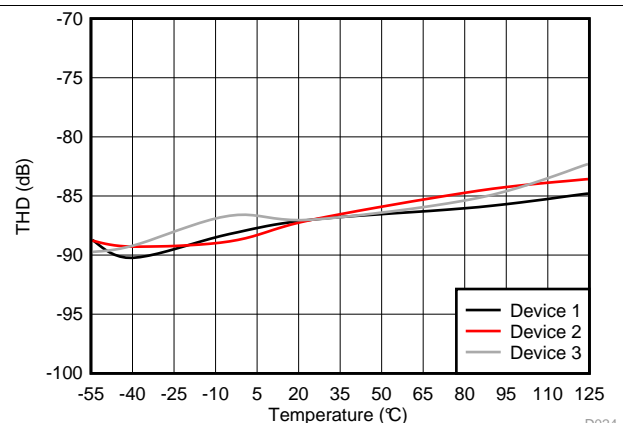
–55°C ≤ T<sub>A</sub> < –40°C for the AMC1311B only

**Figure 25. Nonlinearity vs Temperature**



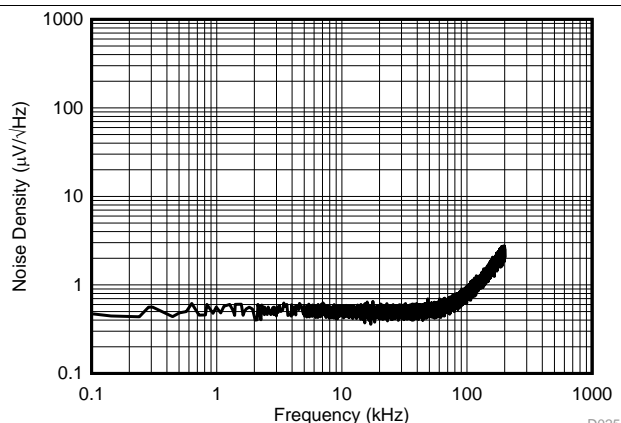
3.0 V ≤ VDD1 < 4.5 V for the AMC1311B only

**Figure 26. Total Harmonic Distortion vs Supply Voltage**



–55°C ≤ T<sub>A</sub> < –40°C for the AMC1311B only

**Figure 27. Total Harmonic Distortion vs Temperature**

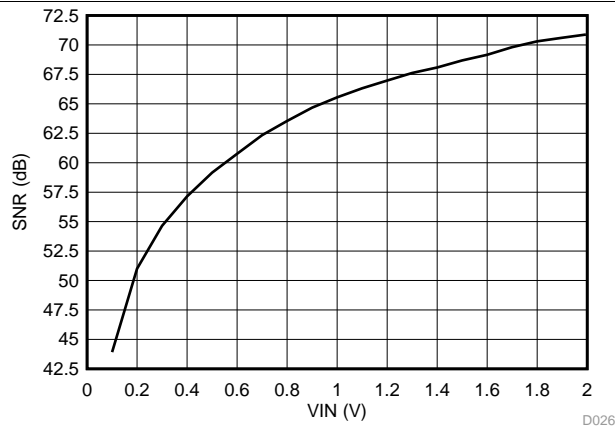


**Figure 28. Input-Referred Noise Density vs Frequency**

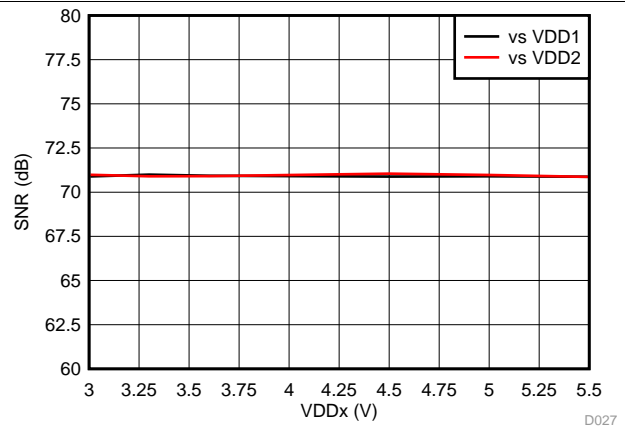


## Typical Characteristics (continued)

at VDD1 = 5 V, VDD2 = 3.3 V, SHTDN = 0 V,  $f_{IN} = 10$  kHz, and BW = 100 kHz (unless otherwise noted)

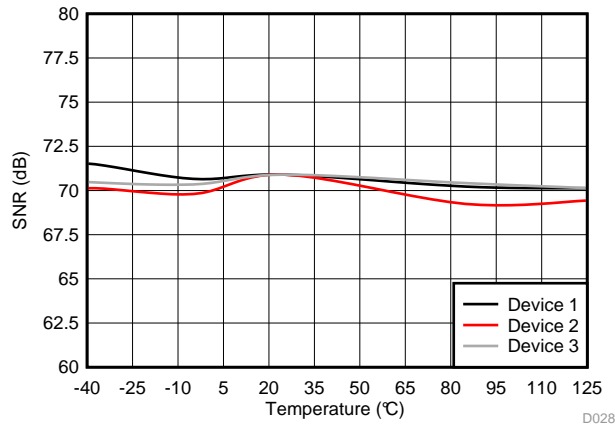


**Figure 29. Signal-to-Noise Ratio vs Input Voltage**



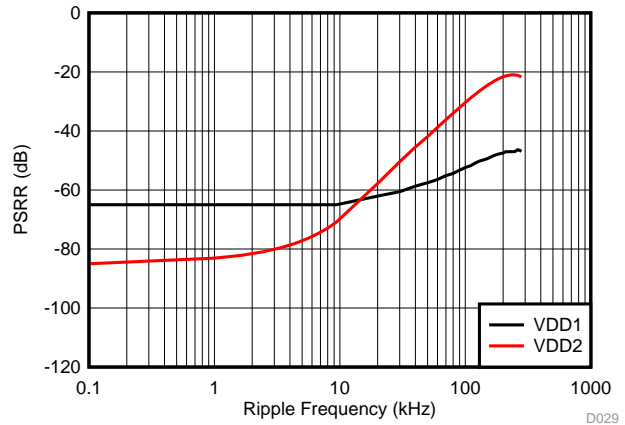
3.0 V ≤ VDD1 < 4.5 V for the AMC1311B only

**Figure 30. Signal-to-Noise Ratio vs Supply Voltage**



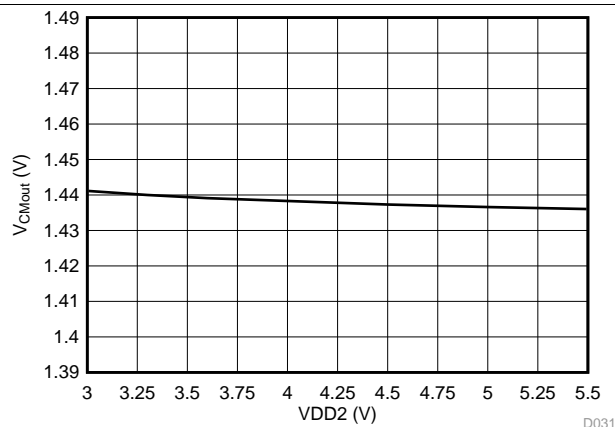
-55°C ≤ T<sub>A</sub> < -40°C for the AMC1311B only

**Figure 31. Signal-to-Noise Ratio vs Temperature**

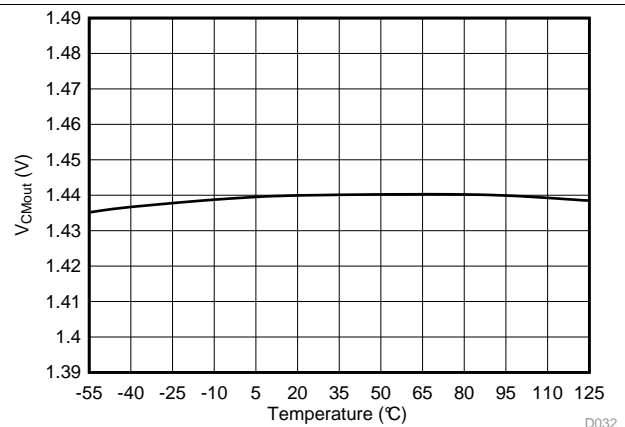


100-mV ripple

**Figure 32. Power-Supply Rejection Ratio vs Ripple Frequency**



**Figure 33. Output Common-Mode Voltage vs Low-Side Supply Voltage**



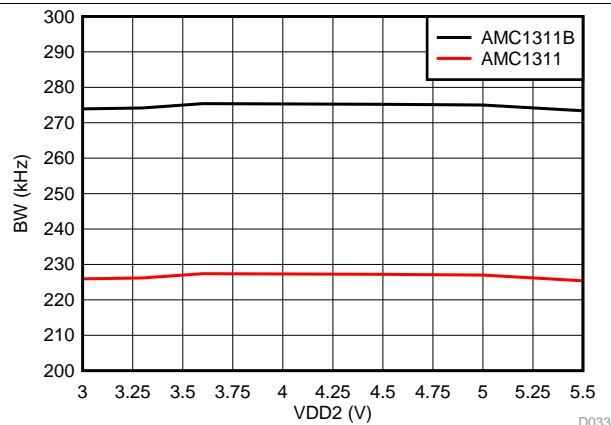
-55°C ≤ T<sub>A</sub> < -40°C for the AMC1311B only

**Figure 34. Output Common-Mode Voltage vs Temperature**

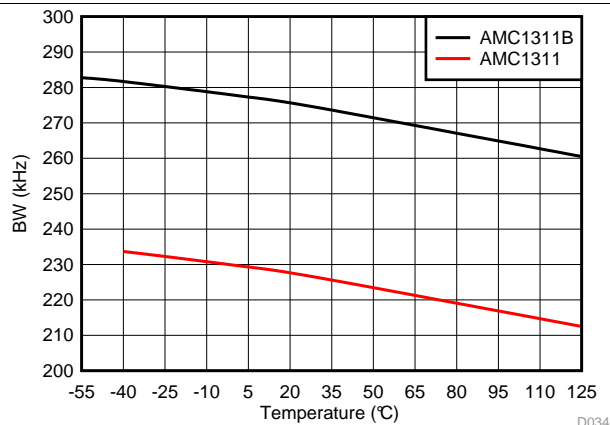


## Typical Characteristics (continued)

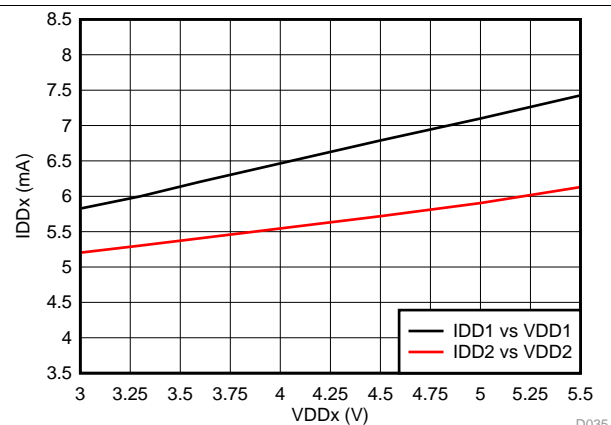
at VDD1 = 5 V, VDD2 = 3.3 V, SHTDN = 0 V,  $f_{IN} = 10$  kHz, and BW = 100 kHz (unless otherwise noted)



**Figure 35. Output Bandwidth vs Low-Side Supply Voltage**

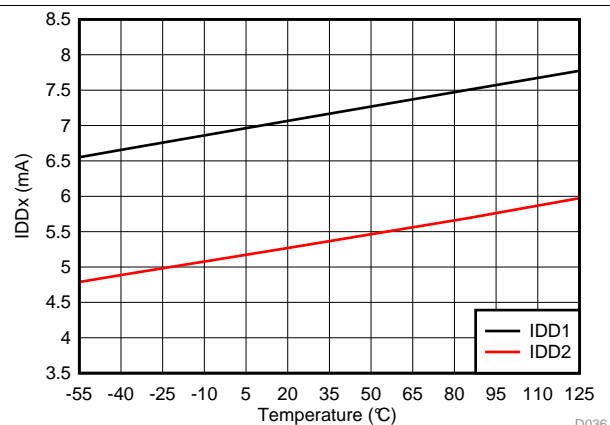


**Figure 36. Output Bandwidth vs Temperature**



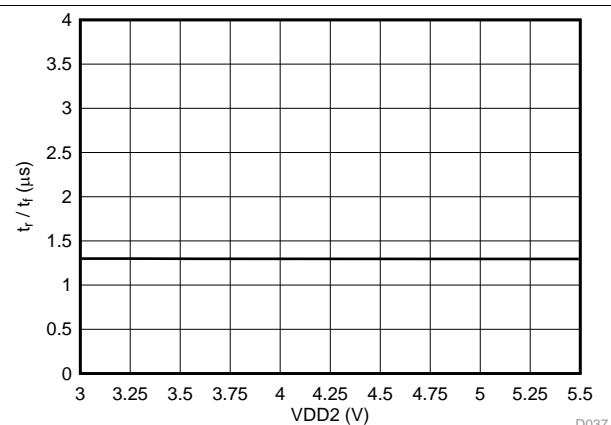
3.0 V ≤ VDD1 < 4.5 V for the AMC1311B only

**Figure 37. Supply Current vs Supply Voltage**

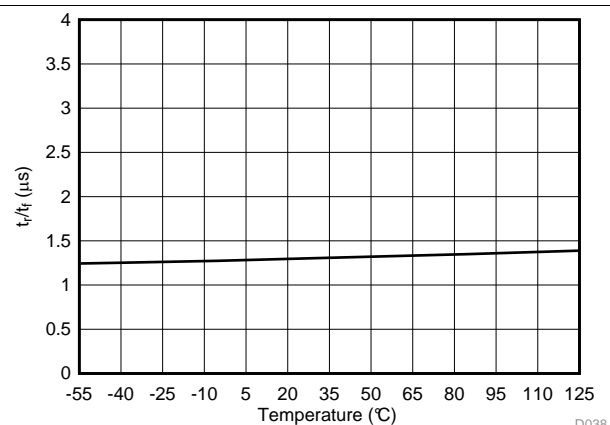


–55°C ≤ T<sub>A</sub> < –40°C for the AMC1311B only

**Figure 38. Supply Current vs Temperature**



**Figure 39. Output Rise and Fall Time vs Low-Side Supply Voltage**



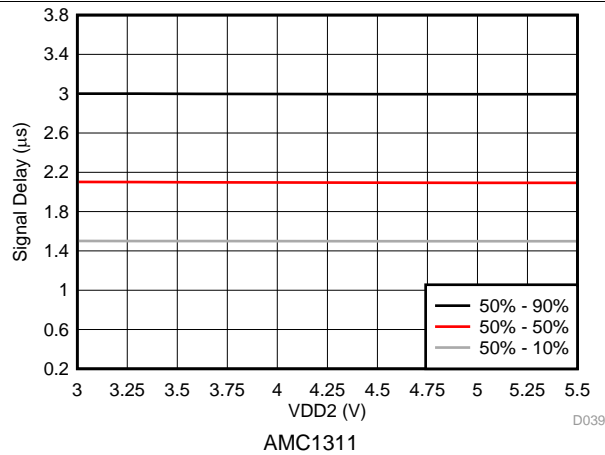
–55°C ≤ T<sub>A</sub> < –40°C for the AMC1311B only

**Figure 40. Output Rise and Fall Time vs Temperature**

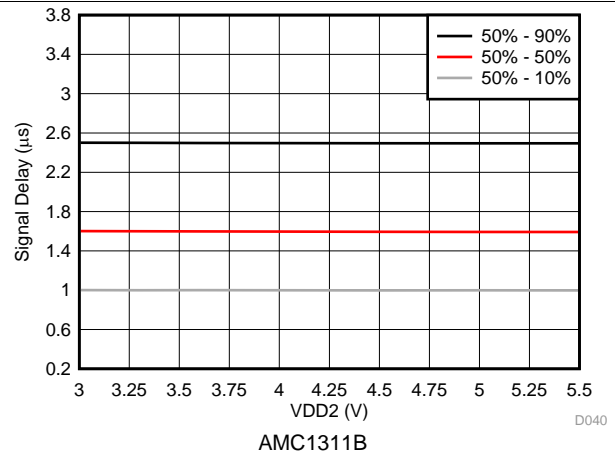


## Typical Characteristics (continued)

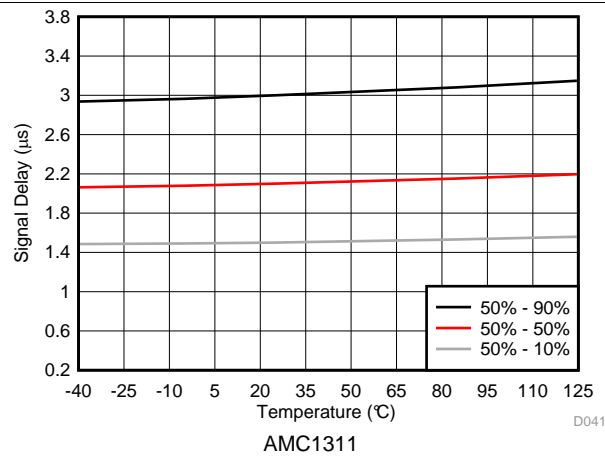
at VDD1 = 5 V, VDD2 = 3.3 V, SHTDN = 0 V,  $f_{IN}$  = 10 kHz, and BW = 100 kHz (unless otherwise noted)



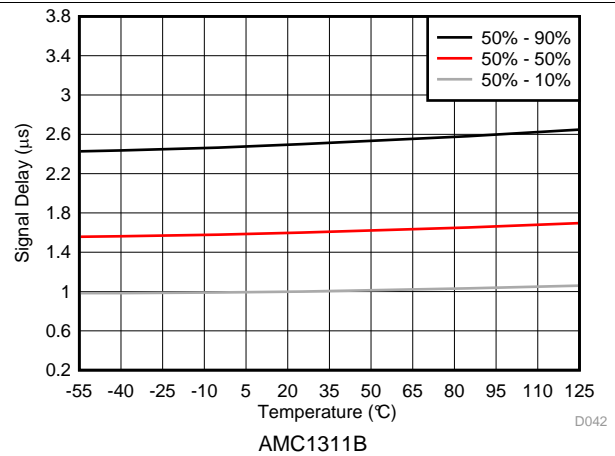
**Figure 41. VIN to VOUTP, VOUTN Signal Delay vs Low-Side Supply Voltage**



**Figure 42. VIN to VOUTP, VOUTN Signal Delay vs Low-Side Supply Voltage**



**Figure 43. VIN to VOUTP, VOUTN Signal Delay vs Temperature**



**Figure 44. VIN to VOUTP, VOUTN Signal Delay vs Temperature**



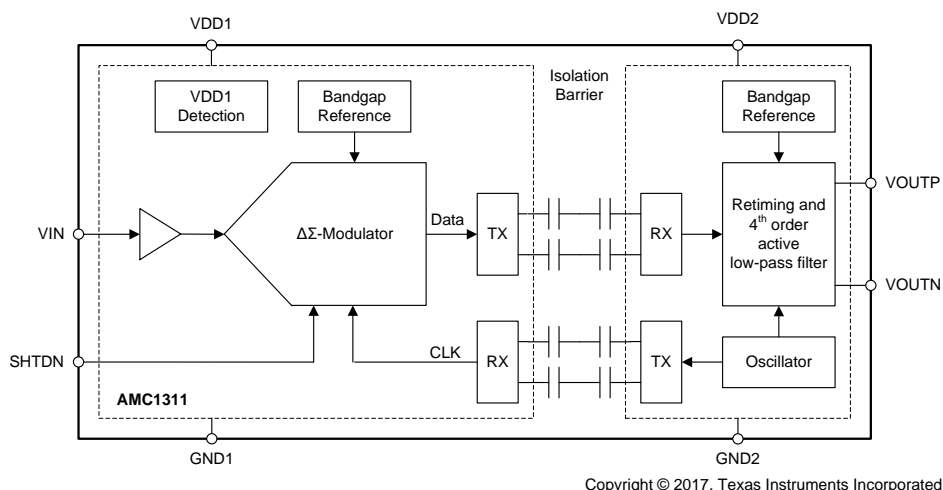
## 8 Detailed Description

### 8.1 Overview

The AMC1311 is a precision, isolated amplifier with a high input-impedance and wide input-voltage range. The input stage of the device drives a second-order, delta-sigma ( $\Delta\Sigma$ ) modulator. The modulator uses the internal voltage reference and clock generator to convert the analog input signal to a digital bitstream. The drivers (termed TX in the [Functional Block Diagram](#) section) transfer the output of the modulator across the isolation barrier that separates the high-side and low-side voltage domains. The received bitstream and clock are synchronized and processed by a fourth-order analog filter on the low-side and presented as a differential analog output.

The SiO<sub>2</sub>-based, double-capacitive isolation barrier supports a high level of magnetic field immunity, as described in [ISO72x Digital Isolator Magnetic-Field Immunity](#). The digital modulation used in the AMC1311 and the isolation barrier characteristics result in high reliability and common-mode transient immunity.

### 8.2 Functional Block Diagram



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### 8.3 Feature Description

#### 8.3.1 Analog Input

The input stage of the AMC1311 feeds a second-order, switched-capacitor, feed-forward  $\Delta\Sigma$  modulator. The modulator converts the analog signal into a bitstream that is transferred over the isolation barrier, as described in the [Isolation Channel Signal Transmission](#) section. The high-impedance, and low bias-current input of the AMC1311 makes the device suitable for isolated voltage sensing applications. [Figure 45](#) depicts the equivalent input structure of the AMC1311 with the relevant components.

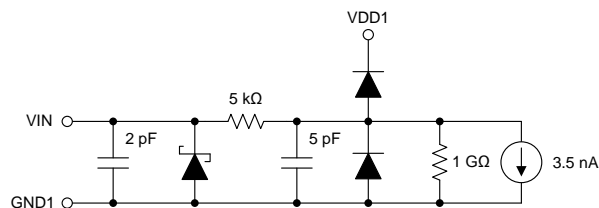


Figure 45. Equivalent Analog Input Circuit

There are two restrictions on the analog input signal, VIN. First, if the input voltage VIN exceeds the voltage of 6.5 V, the input current must be limited to 10 mA because the device input electrostatic discharge (ESD) protection turns on. In addition, the linearity and noise performance of the device are ensured only when the analog input voltage remains within the specified linear full-scale range (V<sub>FSR</sub>).

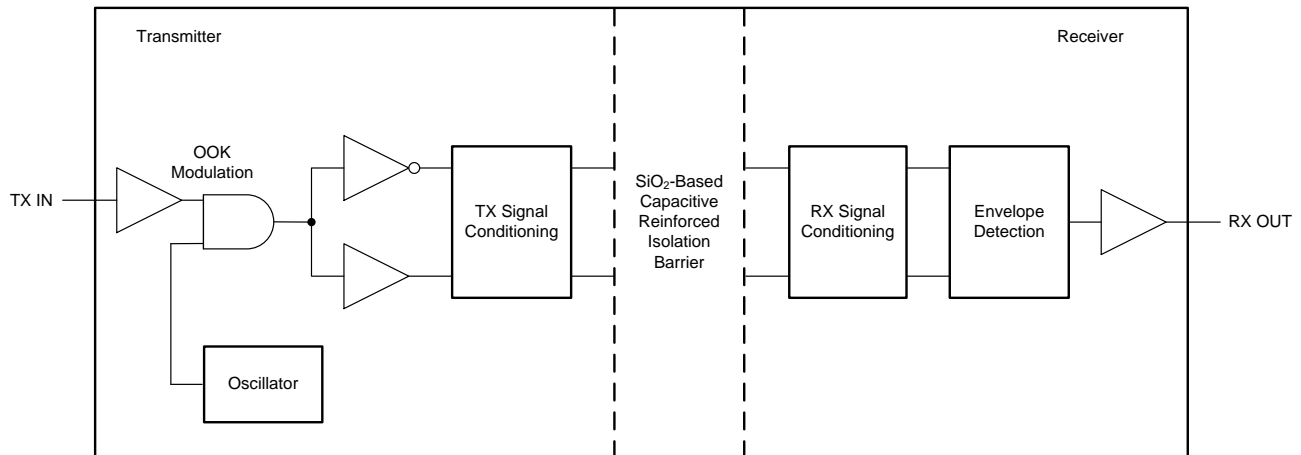


## Feature Description (continued)

### 8.3.2 Isolation Channel Signal Transmission

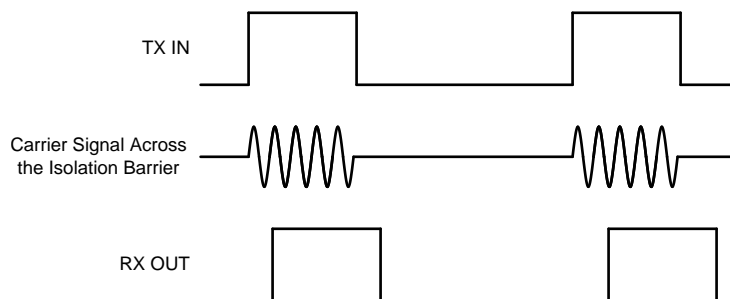
The AMC1311 uses an on-off keying (OOK) modulation scheme to transmit the modulator output bitstream across the SiO<sub>2</sub>-based isolation barrier. As shown in Figure 46, the transmitter modulates the bitstream at TX IN with an internally-generated, high-frequency carrier across the isolation barrier to represent a digital *one* and does not send a signal to represent the digital *zero*. The nominal frequency of the carrier used inside the AMC1311 is 480 MHz.

The receiver demodulates the signal after advanced signal conditioning and produces the output. The AMC1311 also incorporates advanced circuit techniques to maximize the CMTI performance and minimize the radiated emissions caused by the high-frequency carrier and IO buffer switching.



**Figure 46. Block Diagram of an Isolation Channel**

Figure 47 shows the concept of the OOK scheme.



**Figure 47. OOK-Based Modulation Scheme**



## Feature Description (continued)

### 8.3.3 Fail-Safe Output

The AMC1311 offers a fail-safe output that simplifies diagnostics on system level. The fail-safe output is active in three cases:

- When the high-side supply VDD1 of the AMC1311 device is missing
- When the high-side supply VDD1 falls under the  $VDD1_{UV}$  undervoltage threshold level or
- When the SHTDN pin is pulled high

Figure 48 shows the fail-safe output of the AMC1311 that is a negative differential output voltage that does not occur under normal device operation. As a reference value for the fail-safe detection on a system level, use the  $V_{FAILSAFE}$  voltage as specified in the [Electrical Characteristics](#) table.

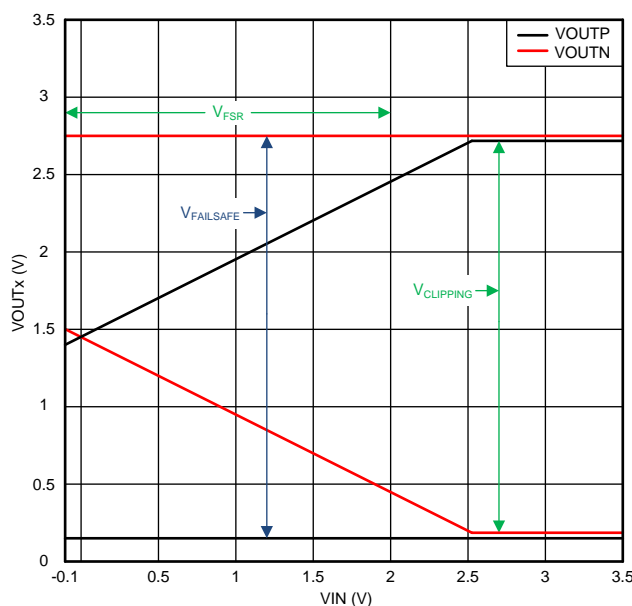


Figure 48. AMC1311 Output Behavior

## 8.4 Device Functional Modes

The AMC1311 is operational when the power supplies VDD1 and VDD2 are applied, as specified in the [Recommended Operating Conditions](#) table.



## 9 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

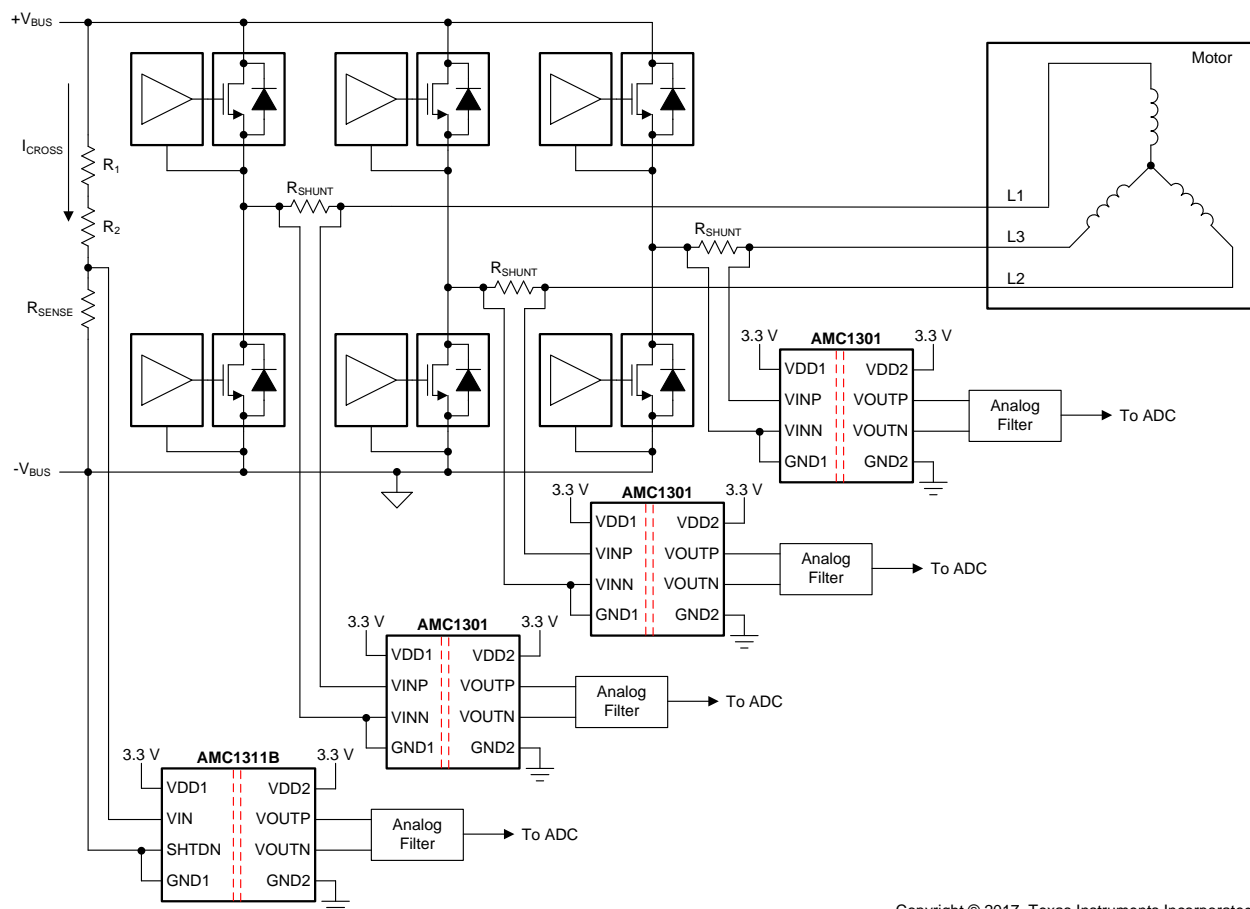
### 9.1 Application Information

The very low input bias current, ac and dc errors, and temperature drift make the AMC1311 a high-performance solution for industrial applications where voltage measurement with high common-mode levels is required.

### 9.2 Typical Application

Isolated amplifiers are widely used in frequency inverters that are critical parts of industrial motor drives, photovoltaic inverters, uninterruptible power supplies, and other industrial applications. The input structure of the AMC1311 is tailored for isolated voltage sensing using resistive dividers to reduce the high common-mode voltage.

Figure 49 illustrates a typical use of the AMC1311 for dc bus voltage sensing in a frequency inverter application. Phase current measurement is accomplished through the shunt resistors,  $R_{SHUNT}$  (in this case, two-pin shunts) and the AMC1301 isolated amplifiers that are optimized for isolated current sensing. The high-impedance input and the high common-mode transient immunity of the AMC1311 ensure reliable and accurate operation even in high-noise environments, such as the power stage of frequency inverters as used in motor drives.



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**Figure 49. Using the AMC1311B for DC Bus Voltage Sensing in Frequency Inverters**



## Typical Application (continued)

### 9.2.1 Design Requirements

Table 1 lists the parameters for this typical application.

**Table 1. Design Requirements**

PARAMETER	VALUE
High-side supply voltage	3.3 V or 5 V
Low-side supply voltage	3.3 V or 5 V
Voltage drop across the sensing resistor for a linear response	2 V (maximum)
Current through the resistive divider, $I_{CROSS}$	0.1 mA (maximum)
Signal delay (50% $V_{IN}$ to 90% $V_{OUTP}$ , $V_{OUTN}$ )	3 $\mu$ s (maximum)

### 9.2.2 Detailed Design Procedure

Use Ohm's Law to calculate the minimum total resistance of the resistive divider to limit the cross current to the desired value ( $R_{TOTAL} = V_{BUS} / I_{CROSS}$ ) and the required sense resistor value to be connected to the AMC1311 input:  $R_{SENSE} = V_{FSR} / I_{CROSS}$ .

Consider the following two restrictions to choose the proper value of the shunt resistor  $R_{SENSE}$ :

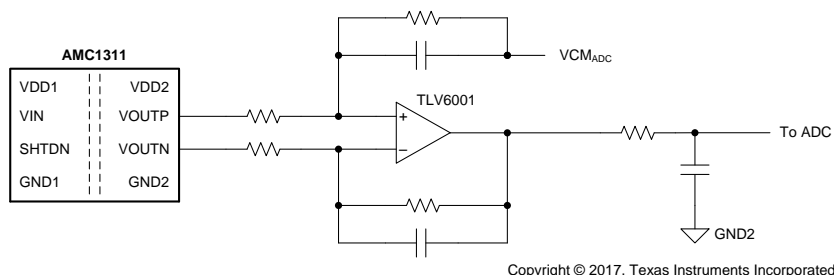
- The voltage drop on  $R_{SENSE}$  caused by the nominal voltage range of the system must not exceed the recommended input voltage range:  $V_{SENSE} \leq V_{FSR}$
- The voltage drop on  $R_{SENSE}$  caused by the maximum allowed system overvoltage must not exceed the input voltage that causes a clipping output:  $V_{SENSE} \leq V_{Clipping}$

Table 2 lists examples of nominal E96-series (1% accuracy) resistor values for systems using 600 V and 800 V on the dc bus.

**Table 2. Resistor Value Examples**

PARAMETER	600-V DC BUS	800-V DC Bus
Resistive divider resistor $R_1$	3.01 M $\Omega$	4.22 M $\Omega$
Resistive divider resistor $R_2$	3.01 M $\Omega$	4.22 M $\Omega$
Sense resistor $R_{SENSE}$	20 k $\Omega$	21 k $\Omega$
Resulting current through resistive divider $I_{CROSS}$	99.3 $\mu$ A	94.5 $\mu$ A
Resulting voltage drop on sense resistor $V_{SENSE}$	1.987 V	1.986 V

For systems using single-ended input ADCs, Figure 50 shows an example of a TLV6001-based signal conversion and filter circuit as used on the AMC1311EVM. Tailor the bandwidth of this filter stage to the bandwidth requirement of the system and use NP0-type capacitors for best performance.



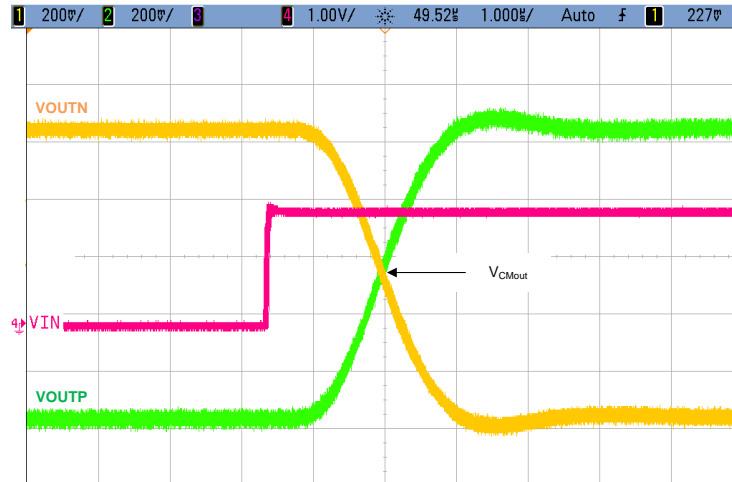
**Figure 50. Connecting the AMC1311 Output to Single-Ended Input ADC**

For more information on the general procedure to design the filtering and driving stages of SAR ADCs, see [18-Bit, 1MSPS Data Acquisition Block \(DAQ\) Optimized for Lowest Distortion and Noise](#) and [18-Bit Data Acquisition Block \(DAQ\) Optimized for Lowest Power](#), available for download at [www.ti.com](http://www.ti.com).



### 9.2.3 Application Curve

In frequency inverter applications, the power switches must be protected in case of an overvoltage condition. To allow for fast system power-off, a low delay caused by the isolated amplifier is required. Figure 51 shows the typical full-scale step response of the AMC1311. Consider the delay of the required window comparator and the MCU to calculate the overall response time of the system.



**Figure 51. Step Response of the AMC1311B**

### 9.3 Do's and Don'ts

Do not leave the analog input VIN of the AMC1311 unconnected (floating) when the device is powered up on the high-side. If the device input is left floating, the bias current may generate a negative input voltage that exceeds the specified input voltage range and the output of the device is invalid.







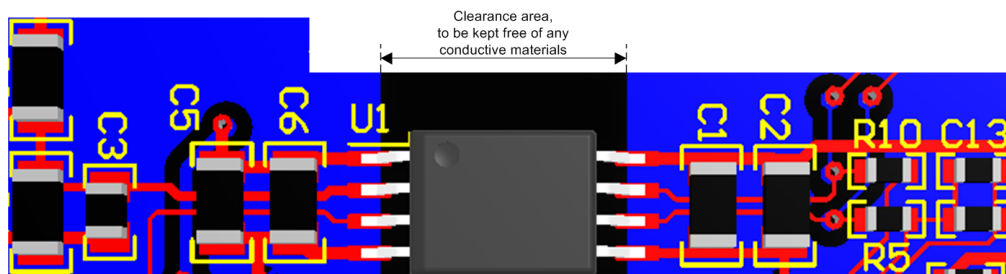
## 11 Layout

### 11.1 Layout Guidelines

For best performance, place the smaller 0.1- $\mu$ F decoupling capacitors (C1 and C6) as close as possible to the AMC1311 power-supply pins, followed by the additional C2 and C5 capacitors with a minimum value of 1  $\mu$ F. The resistors and capacitors used for the analog input (C3) and output filters (R5, R10, and C13) are placed next to the decoupling capacitors. Use 1206-size, SMD-type, ceramic decoupling capacitors and route the traces to the VIN and SHTDN pins underneath. Connect the supply voltage sources in a way that allows the supply current to flow through the pads of the decoupling capacitors before powering the AMC1311.

[Figure 53](#) shows this approach as implemented on the [AMC1311EVM](#). Capacitors C5 and C6 decouple the high-side supply VDD1 while capacitors C1 and C2 are used to support the low-side supply VDD2 of the AMC1311.

### 11.2 Layout Example



**Figure 53. Recommended Layout of the AMC1311**



## 12 Device and Documentation Support

### 12.1 Documentation Support

#### 12.1.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

#### 12.1.2 Related Documentation

For related documentation, see the following:

- [Isolation Glossary](#)
- [Dual, 1MSPS, 16-/14-/12-Bit, 4x2 or 2x2 Channel, Simultaneous Sampling Analog-to-Digital Converter](#)
- [Semiconductor and IC Package Thermal Metrics](#)
- [ISO72x Digital Isolator Magnetic-Field Immunity](#)
- [AMC1301 Precision,  \$\pm 250\$ -mV Input, 3- \$\mu\$ s Delay, Reinforced Isolated Amplifier](#)
- [TLV600x Low-Power, Rail-to-Rail In/Out, 1-MHz Operational Amplifier for Cost-Sensitive Systems](#)
- [AMC1311EVM Users Guide](#)
- [18-Bit, 1-MSPS Data Acquisition Block \(DAQ\) Optimized for Lowest Distortion and Noise](#)
- [18-Bit, 1-MSPS Data Acquisition Block \(DAQ\) Optimized for Lowest Power](#)
- [SN6501 Transformer Driver for Isolated Power Supplies](#)

### 12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to order now.

**Table 3. Related Links**

PARTS	PRODUCT FOLDER	ORDER NOW	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
AMC1311	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
AMC1311B	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>

### 12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 12.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 12.5 Trademarks

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.



## 12.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 12.7 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, And Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.



## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
AMC1311BDWV	ACTIVE	SOIC	DWV	8	64	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-55 to 125	1311B	<a href="#">Samples</a>
AMC1311BDWVR	ACTIVE	SOIC	DWV	8	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-55 to 125	1311B	<a href="#">Samples</a>
AMC1311DWV	ACTIVE	SOIC	DWV	8	64	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	1311	<a href="#">Samples</a>
AMC1311DWVR	ACTIVE	SOIC	DWV	8	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	1311	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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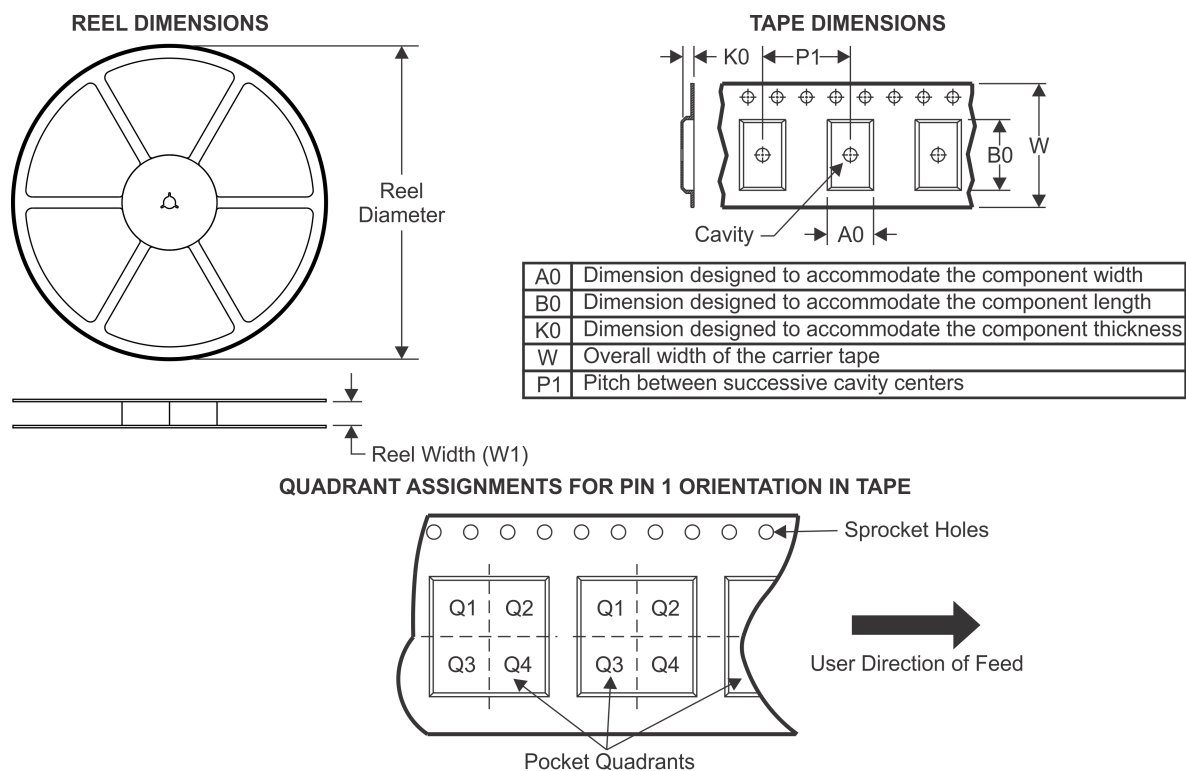


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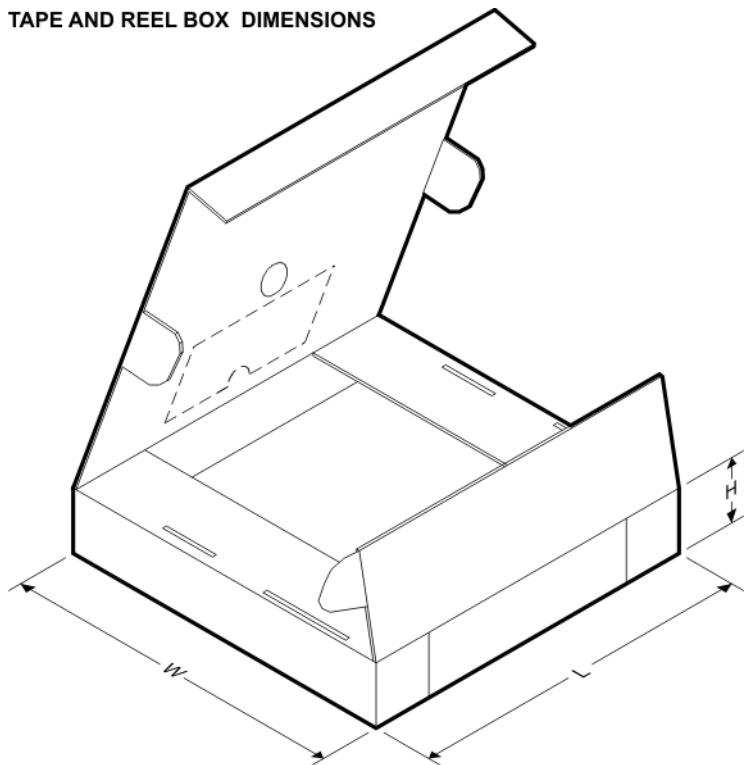
**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
AMC1311BDWVR	SOIC	DWV	8	1000	330.0	16.4	12.05	6.15	3.3	16.0	16.0	Q1
AMC1311DWVR	SOIC	DWV	8	1000	330.0	16.4	12.05	6.15	3.3	16.0	16.0	Q1



## TAPE AND REEL BOX DIMENSIONS



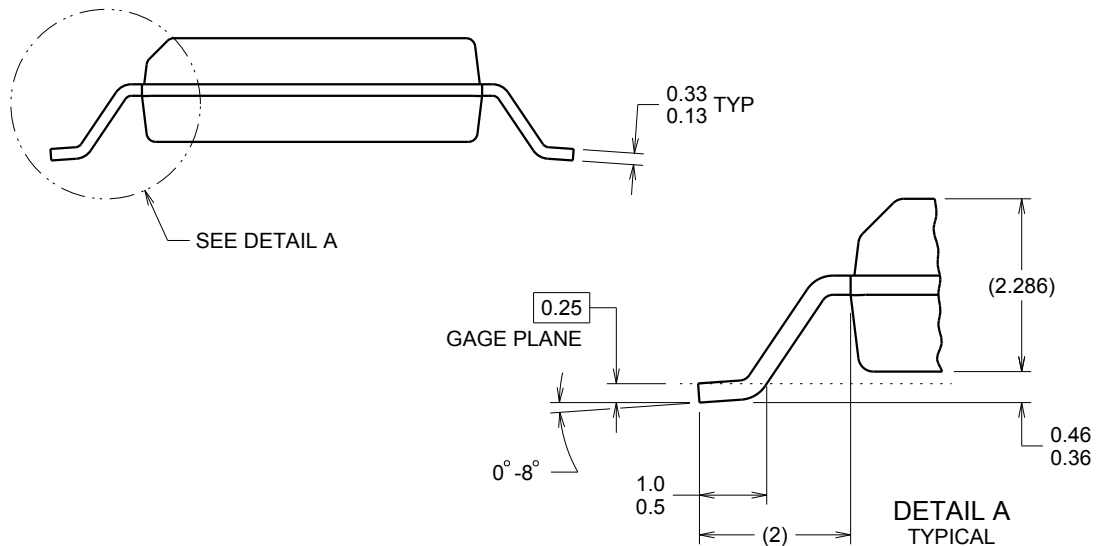
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
AMC1311BDWVR	SOIC	DWV	8	1000	367.0	367.0	38.0
AMC1311DWVR	SOIC	DWV	8	1000	367.0	367.0	38.0



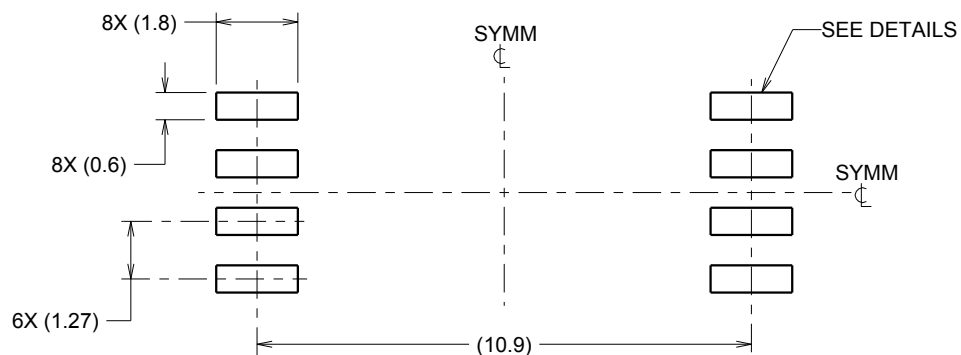
SOIC - 2.8 mm max height

PIN 1 ID AREA  
 11.5 ± 0.25 TYP  
 5.95  
 5.75  
 NOTE 3  
 1  
 4  
 8  
 5  
 6X 1.27  
 2X 3.81  
 8X 0.51  
 0.31  
 7.6  
 7.4  
 NOTE 4  
 A  
 B  
 SEATING PLANE  
 0.1 C  
 2.8 MAX  
 C  
 A  
 B

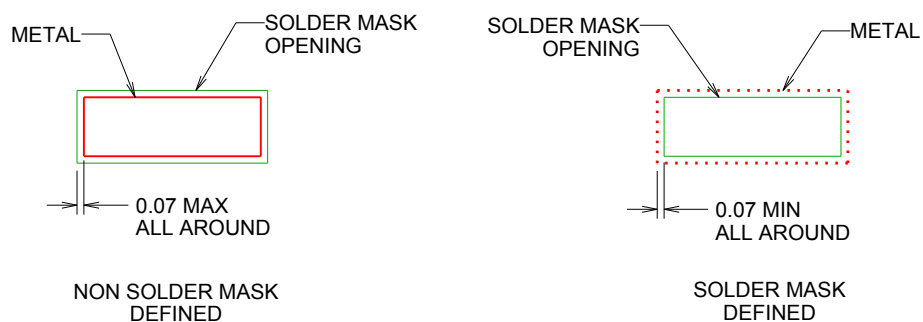


1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.





LAND PATTERN EXAMPLE  
9.1 mm NOMINAL CLEARANCE/CREEPAGE  
SCALE:6X



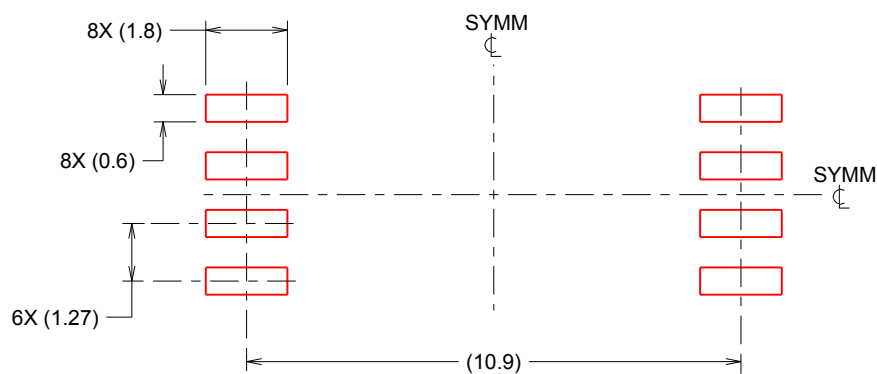
SOLDER MASK DETAILS

4218796/A 09/2013

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





SOLDER PASTE EXAMPLE  
 BASED ON 0.125 mm THICK STENCIL  
 SCALE:6X

4218796/A 09/2013

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.



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